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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/675,170	09/30/2003	David Arnold Luick	ROC920030255US1	5915

7590 12/27/2005

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EXAMINER	
GU, SHAWN X	

ART UNIT	PAPER NUMBER
2189	

DATE MAILED: 12/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/675,170	LUICK, DAVID ARNOLD	
	Examiner	Art Unit	
	Shawn Gu	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,9-14 and 17-21* is/are rejected.

7)☒ Claim(s) *6-8,12, 15 and 16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

The disclosure is objected to because of the following informalities:

The specification contains numerous omissions of serial numbers referenced by the Applicant, such as those on Pages 1 and 7 of the specification.

Appropriate correction is required.

Claim Objections

Claim 12 is objected to because of the following informalities: the second appearance of the word "execution" should be spelled "executing". Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1, 12, and 14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As for claim 1, it is unclear to the Examiner if the "a location more accessible" to is more accessible to the said processor than the memory, or some other entity. The Examiner is rejecting the claim in light for the former interpretation. Appropriate correction is required.

As for claim 12, the claim recites the limitations "said plurality of sub-units of a segment" and "said at least one structure for temporarily storing data". There is insufficient antecedent basis for these limitations in the claim. Appropriate correction is required.

As for claim 14, it is unclear to the Examiner whether the up-or-down counters are maintained "automatically" from which entity that might have controlled it if it weren't maintained "automatically". Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 5, 9-12, 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Doing et al. [6,161,166] (hereinafter "Doing"), in further view of Kedem et al. [6,134,643] (hereinafter "Kedem"), Schumann et al. [6,012,106] (hereinafter "Schumann"), and "Operating Systems" [Tanenbaum and Woodhull] (hereinafter "Tanenbaum").

As for claim 1, Doing teaches a digital data processing device, comprising:

a memory (Fig 1A and Fig 1B, 102 Main Memory), said memory containing a page table, said page table having a plurality of page table entries corresponding to respective pages in a first address space (Fig 8, 822 Page Table);

at least one processor (Fig 1A and Fig 2, 101 CPU); and

at least one structure for temporarily storing data from said memory in a location more accessible to said processor (Fig 1A, 108 L2 cache). Doing does not teach a pre-fetch engine or pre-fetch data contained in each page table entry.

However, Kedem teaches a digital data processing device which comprises a pre-fetch engine (Fig 1, combination of 30 Prefetch Controller, 40 Prediction Table, and 35 Prefetch Buffer), said pre-fetch engine pre-fetching data from memory pages to at least one structure for temporarily storing data from said memory in a location more accessible to said processor using pre-fetch data (Col 3, Lines 22-42), in order to improve access latency without significantly affecting the operation of the processor (Col 3, Lines 10-21). Therefore, it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention that Doing digital data processing device

could incorporate Kedem's pre-fetch engine and pre-fetch data to improve access latency. Yet, Kedem does not teach that the pre-fetch data used by the pre-fetch engine is contained in each of a plurality of said page table entries to identify a plurality of sub-units of the corresponding page as pre-fetch candidates..

However, Schumann teaches a digital data processing device which comprises pre-fetching data from memory pages using pre-fetch data with respect to the corresponding memory page, the pre-fetch data contained in a plurality of page table entries in a page table, the pre-fetch data identifying a plurality of sub-units (cache lines) of the corresponding page as pre-fetch candidates (Fig 2, Prefetch Length in 21 Page Table; Col 4, Lines 18-63), with the intention to reduce the number of wait states and improve access time (see Abstract), and further improve cache throughput (Col 1, Lines 60-65). Furthermore, keeping the pre-fetch data in cache as disclosed in Kedem increases design complexity since that further require deciding the size of the prediction table and replacement algorithm (Kedem, Col 3, Lines 43-49). Therefore, it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention that Doing device in combination with that of Kedem's, would reduce number of wait states, improve access time and cache throughput, and further reduce design complexity, if further includes Schumann's design. Yet, the combined references above teach a page table with a plurality of page table entries instead of a segment table with a plurality of segment table entries.

However, Tanenbaum teaches that segmentation is a similar method to paging for virtual memory systems (Pages 343-351) which offers the advantages of simplifying

the handling of data structures that grow and shrink in size, and the linking of procedures (Page 346), and therefore it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention that Tanenbaum's segment table with a plurality of segment table entries would be combined with the references above in order to provide a virtual memory system with the mentioned benefits.

As for claim 5, Doing already substantially discloses the claim as described above, in further view of Kedem, Schumann, and Tanenbaum, and Schumann further teaches that the said pre-fetch data is automatically generated by the digital data processing device (Schumann, Col 4, Lines 55-63).

As for claim 9, Doing already substantially discloses the claim as described above, in further view of Kedem, Schumann, and Tanenbaum, and further teaches that the said segment table translates segment identifiers in an effective address space of an executing task to segment identifiers in a global virtual address space, and wherein a page table translates segment identifiers in the global virtual address space to pages in said memory (Doing, Fig 8).

As for claims 10, 11, 17, and 18, Doing already substantially discloses the claim as described above, in further view of Kedem, Schumann, and Tanenbaum, and further teaches that said pre-fetch action is performed responsive to an occurrence of an event of a first type, wherein said event of said first type comprises generating a reference to

data within the corresponding segment (Schumann, Col 4, Lines 55-63 and Lines 18-25). The benefit for the combined teachings is congruent with the reason to combine as cited in claim 1's rejection.

As for claim 12, Doing already substantially discloses the claim as described above, in further view of Kedem, Schumann, and Tanenbaum, and further teaches an instruction unit determining instruction sequences (Fig 2, 201 Instruction Unit) and an execution unit execution instructions in said instruction sequences (Fig 2, 211 Execution Unit).

As for claim 19, Doing already substantially discloses the claim as described above, in further view of Kedem, Schumann, and Tanenbaum. The pre-fetched sub-units (cache lines) of the segment are associated to the segment by the Prefetch_Length value taught by Schumann as described above.

Claims 2-4,13, 20, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Doing in combination with Kedem, Schumann, and Tanenbaum, in further view of "Computer Architecture A Quantitative Approach" [by David A. Patterson and John L. Hennessy] (hereinafter "Patterson") and Chauvel [US 6,957,315 B2] (hereinafter "Chauvel").

As for claims 2, 3, and 13, Doing already substantially discloses the claim as described above, in further view of Kedem, Schumann, and Tanenbaum, but does not particularly point out that the said pre-fetch action comprises pre-fetching address translation data with respect to said sub-unit into at least one address translation cache structure, wherein said at least one address translation cache structure comprises a translation look-aside buffer. However, Patterson discloses that in a virtual memory system such as that of Doing's, a TLB (Translation Look-aside Buffer) that contains address translation data is included to improve address translation latency (Pages 445-446). Chauvel further teaches pre-fetching TLB entries to prevent TLB misses (Col 8, Lines 18-22).

Therefore it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention that Patterson and Chauvel's teachings can be combined with those of Doing, Kedem, Schumann, and Tanenbaum, in order to improve address translation latency and prevent TLB misses.

As for claim 4, Doing already substantially discloses the claim as described above, in further view of Kedem, Schumann, and Tanenbaum, and further teaches that the said at least one address translation cache structure comprises an effective-to-real address translation table (ERAT) (Figs 4-8).

As for claims 20 and 21, the claims are already substantially disclosed as described above in the rejections for claims 2, 3, 13, and 19.

Allowable Subject Matter

Claims 6-8, 15, and 16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 14 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shawn Gu whose telephone number is (571) 272-0703. The examiner can normally be reached on 9am-5pm, Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571)272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shawn X Gu
Assistant Examiner
Art Unit 2189

21 December 2005